REMARKS

Claims 1-8 are presently pending in the application. Claim 9 has been withdrawn from consideration as being directed to a non-elected invention. Reconsideration and allowance of all claims are respectfully requested in view of the following remarks.

Claims 1-8 were objected to by the Examiner due to informalities. Claim 1 has been amended to correct the misspelled word "pattering" to --patterning--. Accordingly, the Examiner's objection to Claim 1, and Claims 2-7, which depend from Claim 1, have been obviated.

The Examiner has rejected Claims 1-2 and 5-6 under 35 U.S.C. §102(e) as being anticipated by Kim et al. Claims 3 and 8 were rejected by the Examiner under 35 U.S.C. §103(a) as being unpatentable over Kim et al. Further, Claims 4 and 7 were rejected under 35 U.S.C. 103 as being unpatentable over Kim et al. in view of Lin et al. For the following reasons, the prior art rejections are respectfully traversed.

The Applicant respectfully submits that Kim et al. fails to teach the steps of forming a metal layer over a substrate; forming a pad oxide layer over the metal layer; and patterning and etching the pad oxide layer and metal layer sequentially to form interconnect lines over the substrate, as recited in Claim 1.

The Applicant respectfully points out the Examiner that the claims recited that the metal layer must be formed on the substrate, and then the pad oxide layer and the metal layer must be patterned and etched together in one step.

In contrast, FIG. 1 of Kim et al. show a cross-sectional view of an integrated circuit topology having an insulating layer 104 and patterned spaced conductors 106. The conductors 106 are a spaced conductive pattern or metal interconnections, not an

un-etched metal layer. Kim et al. clearly state that the conductors 106 have a height of about 1 microns to 1.2 microns and the distance between the conductors 106 can be about 0.8 microns to 0.9 microns.

However, Kim et al. fail to teach the steps of forming a metal layer over a substrate, forming a pad oxide layer over the metal layer, and patterning and etching the pad oxide layer and metal layer sequentially to form interconnect lines over the substrate.

The first layer 108 of the multilayer dielectric in Kim et al. is formed over the conductors 106 after the conductors 106 are formed. Moreover, the first layer 108 of the multilayer dielectric is never etched in the teaching of Kim et al. FIG. 2 of Kim et al. only show that the first layer 108 of the multilayer dielectric covers the conductors 106 with purposely poor step coverage. Kim et al. do not teach or suggest a step of patterning and etching the conductors 106 and the first layer 108 of the multilayer dielectric together.

The Applicant points out to the Examiner that the steps recited must be taken in turn, and that the conductors 106 in Kim et al. must be formed on the intermetal dielectric layer 104 firstly and then the first layer 108 of the multilayer dielectric is formed to cover the conductors 106 with purposely poor step coverage, while no patterning or etching process are performed.

Kim et al. do not teach or suggest each and every limitation of Claim 1. MPEP §2131 states: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."

Since Kim et al. do not teach or suggest each and every limitation of Claim 1, Claim 1 is not anticipated by, nor obvious over Kim et al., and the rejection of Claim 1 under 35

U.S.C. §102(e) should be withdrawn.

With respect to Claims 4 and 7, the Applicant respectfully submits that neither Kim et al. nor Lin et al. teaches or suggests the recitations of those claims.

Rather, Lin et al., on whom the Examiner relies, teaches a method for air gaps in multilevel interconnection similar to that of Kim et al. Particularly, as shown in FIGS. 1 and 2 of Lin et al., the interconnect pattern 12 is formed by patterning on the insulating layer 10 before the layer 14 is formed thereover. The interconnect pattern 12 is a spaced conductive pattern or metal interconnections just like the conductors 106 of Kim et al., and not an un-etched metal layer. Lin et al. actually fails to teach the steps of forming a metal layer over a substrate, forming a pad oxide layer over the metal layer, and patterning and etching the pad oxide layer and metal layer sequentially to form interconnect lines over the substrate.

Accordingly, since Lin et al. fail to make up for the deficiencies in Kim et al., Claims 4 and 7 are not obvious over either the individual or the combination of the Kim et al. and Lin et al. references, and the rejection of Claims 4 and 7 under 35 U.S.C. §103 should be withdrawn.

Further, since Claims 1-8 depend from Claim 1, they are also patentably distinguishable over the applied prior art for the reasons cited above with respect to Claim 1.

Accordingly, the present application should be in form for allowance and such action is hereby solicited.

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 04-1061.

Respectfully submitted,

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